

REMARKS

Claims 1-3 are cancelled without prejudice. Claims 4, 5 and 7-11 are presently pending and stand rejected.

Claims 4 and 5 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ben-Yoseph. Claim 4 is amended to include, among other limitations, "wherein a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access".

Examiner has indicated that "Ben-[Yoseph] teaches a system incurring delays in subsequent accesses by a device (column 10, lines 4-20). Ben does not explicitly disclose a predetermined delay between subsequent accesses. Robinett teaches a unified memory system wherein a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access (predetermined delay is enforced to allow for sufficient adjustment between subsequence schedules accesses, column 7, lines 50-67)."

Assignee respectfully traverses the rejection. Ben-Yoseph teaches that "A read operation over the system PCI bus 104 involves a substantial delay in comparison to reading the shadow values directly from shadow storage that is local to the host processor." Col. 10, Lines 7-10. Similarly, Robinett merely teaches "The processor schedules each *transport packet* to be outputted in a time slot at a particular dispatch time, corresponding to a predetermined delay in the remultiplexer node." Assignee respectfully submits that the foregoing does not teach does not teach "incurring delays in subsequent accesses by a device".

Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claim 4, and dependent claims 5, and 7-11.

Claim 7 was rejected under 35 U.S.C. § 103(a) as obvious from the combination of Ben-Yoseph in view of Robinette. Claim 7 recites, among other limitations, "a circuit component associated with one or more devices and coupled between the associated devices and the memory request arbiter, wherein the circuit component is used to enforce at least a predetermined minimum interval between subsequent accesses by the associated device to the memory". Examiner has indicated that Robinett, "processor circuit introduces predetermined delay between subsequent accesses.

Even if the transport packets are deemed to be devices, the foregoing in Robinette does not teach "wherein the circuit component is used to enforce at least a predetermined minimum interval between subsequent accesses by the associated device *to the memory*". Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claim 7.

CONCLUSION

For at least the foregoing reasons, Assignee submits that each of the pending claims are now in a condition for allowance. Accordingly, Examiner is requested to pass this case to issuance.

It is believed that all monies for the actions described herein are provided with this correspondence. To the extent that additional monies are required for any of the actions requested in the correspondence, Commissioner

is authorized to charge such fees and credit any overpayments to deposit account 13-0017.

Respectfully Submitted

A handwritten signature in black ink, appearing to read 'MDL', is written over a horizontal line.

Mirut Dalal
Attorney for Assignee
Reg. No. 44,052

Date: May 7, 2009

McAndrews, Held & Malloy, Ltd.
500 West Madison - Suite 3400
Chicago, IL 60661

Phone (312) 775-8000
FAX (312) 775-8100